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10/563,120	01/03/2006	Kohichi Morino	R2184.0472/P472	8029

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DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
O'TOOLE, COLLEEN J	

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2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,120	MORINO ET AL.	
	Examiner	Art Unit	
	COLLEEN O'TOOLE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 December 2007_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-11_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-11_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _2/4/08_.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amended claims 1 and 4-8 and original claims 2-3 and 9-11 are rejected on the grounds below. The amendment to the specification has been reviewed and accepted by the Examiner.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. (U.S. Patent 5,861,771 as recited in the Information Disclosure Statement dated January 3, 2006, hereafter Matsuda) in view of Iravani (U.S. Patent 5,936,460), and further in view of Negoro et al. (JP2002270781A as recited on the Information Disclosure Statement filed January 3, 2006, hereafter Negoro).

Claim 1: Matsuda teaches a semiconductor device (Figure 4) comprising:

a high-breakdown-voltage regulator (7) configured to operate at a high input voltage (Vcc1);

a reference voltage generating circuit (41) structured as a low-breakdown-voltage component (voltage divided VR) and configured to receive an output voltage (VR) from the high-breakdown-voltage regulator (7) to generate a reference voltage (Vref);

a differential amplifier circuit (51) structured as another low-breakdown-voltage component (voltage divided VR) and configured to receive the output voltage (VR) from the high-breakdown-voltage regulator (7) and the reference voltage (Vref) from the reference voltage generating circuit (41) to produce a drive voltage (Vc);

an output driver (63) structured as a high-breakdown-voltage component (via Vcc1) and configured to operated based on the drive voltage (Vc), wherein the output driver is a MOS transistor (column 6 lines 45-46); and

resistors (R3 and R4) connected in series to the output driver (63) to divide an output voltage (Vcc2) of the output driver (63) and feed the divided voltage (Vf) back to the differential amplifier circuit (51).

Matsuda does not teach a constant current inverter circuit. Iravani teaches a constant current circuit (Figure 2) coupled inserted between a power supply line (Vdd corresponding to Vcc1 of Matsuda) and the output driver (Iref2 connected to 61 of Matsuda, which is connected to output driver 63 of Matsuda). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the current source taught by Iravani in the regulator circuit taught by Matsuda to provide a stable, noise-free output current (column 1 lines 16-18, column 3 lines 58-59 of Iravani, where the internal circuits of Matsuda require high precision; column 3 lines 16-21).

Neither Matsuda nor Iravani teach a diode having a reverse breakdown voltage lower than an oxide breakdown voltage of the MOS transistor. Negoro teaches a diode (11; Figure 1) inserted between a gate and a source of the MOS transistor (5

corresponding to 63 of Matsuda), the diode (11) having a reverse breakdown voltage lower than an oxide breakdown voltage of the MOS transistor (Abstract, where the reverse breakdown of the protective diode is about half the gate-oxide-film breakdown voltage of the transistor 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the diode taught by Negoro in the combined circuit taught by Matsuda and Iravani to prevent damage to the gate oxide film of a transistor (Abstract).

Claim 2: Matsuda further teaches that the high-breakdown-voltage output driver (6) and the low-breakdown-voltage components (4 and 5) are MOS transistors with gate oxide films having a first thickness (column 2 lines 41-44).

Claim 3: Matsuda further teaches that the high- breakdown-voltage regulator is structured by a high-breakdown-voltage MOS transistor with a gate oxide film having a second thickness greater than the first thickness (inherent because the size of 4, 5, and 6 are reduced; column 2 lines 41-44).

Claim 4: Matsuda further teaches that the output driver (63; Figure 4) is a P-channel MOS transistor (from Figure 4). Negoro further teaches a diode (11) inserted between the gate and the source of the P-channel MOS transistor (63 of Matsuda) and having a breakdown voltage lower than an oxide breakdown voltage of the P-channel MOS transistor (Abstract).

Claim 5: Claim 5 recites the same limitations as claim 4, but using an N-channel MOS transistor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used an N-channel MOS transistor instead of a P-channel MOS transistor and therefore claim 5 is rejected for the same reasons as claim 4 above. The selection of something based on its known suitability for its intended use has been held to support a *prima facie* case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.,* 325 U.S. 327, 65 USPQ 297 (1945).

Claim 6: The combined circuit further teaches that the output driver (63; Figure 4 of Matsuda) is a P-channel MOS transistor (as seen in Figure 4 of Matsuda) the constant current inverter comprising:

a constant current circuit (Iref2 of Iravani) connected between a power supply line (Vcc1 of Matsuda) and the output driver (63 of Matsuda); and

a MOS transistor (61 of Matsuda) controlled by the drive voltage output (Vc of Matsuda) from the differential amplifier circuit (51 of Matsuda).

Claim 7: Matsuda further teaches that the output driver is a P-channel MOS transistor (63; Figure 4) the constant current inverter (6) comprising:

a first N-channel MOS transistor (61) to which the reference voltage (Vref) generated by the reference voltage generator is supplied (via 51);

a first P-channel MOS transistor (62) connected in series to the first N-channel MOS transistor (61) to produce a constant current (mirrors current from 61);

a second P-channel MOS transistor (63) defining a constant current circuit under a current mirror configuration (mirrors current from 62); and

Matsuda does not explicitly teach a second N-channel MOS transistor to which the drive voltage output from the differential amplifier circuit is supplied. However, it is known in the art to use self-biased MOS transistors to be resistive components R3 and R4. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a second N-channel MOS transistor to drive the voltage output from the differential amplifier for resistor R3. The selection of something based on its known suitability for its intended use has been held to support a *prima facie* case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.,* 325 U.S. 327, 65 USPQ 297 (1945).

Claim 8: Matsuda teaches a semiconductor device (Figure 4) comprising:

a reference voltage generating circuit (41) configured to generate a reference voltage (Vref);

a differential amplifier circuit (51) configured to receive the reference voltage (Vref) and generates a drive voltage (Vc);

an output driver (63) configured to operate based on the drive voltage (Vc), wherein the output driver is a MOS transistor (column 6 lines 45-46);

resistors (R3 and R4) connected in series to the output driver (63) to divide an output voltage (Vcc2) of the output driver (63) and feed the divided voltage (Vf) back to the differential amplifier circuit (51).

Matsuda does not teach a constant current circuit. Iravani teaches a constant current circuit (Figure 2) inserted between a power supply line (Vdd) and a combination of the reference voltage generating circuit (Iref1 connected to Vref of Matsuda) and the differential amplifier circuit (Iref2 connected to 61 of Matsuda). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the current source taught by Iravani in the regulator circuit taught by Matsuda to provide a stable, noise-free output current (column 3 lines 58-59).

Neither Matsuda nor Iravani teach a diode having a reverse breakdown voltage lower than an oxide breakdown voltage of the MOS transistor. Negoro teaches a diode (11; Figure 1) inserted between a gate and a source of the MOS transistor (5 corresponding to 63 of Matsuda), the diode (11) having a reverse breakdown voltage lower than an oxide breakdown voltage of the MOS transistor (Abstract, where the reverse breakdown of the protective diode is about half the gate-oxide-film breakdown voltage of the transistor 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the diode taught by Negoro in the combined circuit taught by Matsuda and Iravani to prevent damage to the gate oxide film of a transistor (Abstract).

Claim 11: Iravani further teaches that the constant current circuit (Figure 2) is structured by multiple MOS transistors connected in series to form a multi-stage constant current circuit (61 of Matsuda is in series with m1 of Iravani).

3. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda, Iravani, and Negoro as applied to claim 8 above, and further in view of Menegoli et al. (U.S. Patent Application Publication 2004/0046532, hereafter Menegoli). Matsuda, Iravani, and Negoro teach the circuit as recited in claim 8 above. Neither Matsuda, Iravani, nor Negoro teaches that the constant current circuit (7; Figure 6) is structured by depression-mode or enhancement mode NMOS or PMOS transistor. Menegoli teaches that MOSFET transistors can be made either enhancement or depletion by adjusting the surface concentration of the channel region. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used enhancement or depletion mode NMOS or PMOS transistors to adjust the threshold of the NMOS or PMOS transistors ([0020]).

Response to Arguments

4. Applicant's arguments filed December 28, 2007 have been fully considered but they are not persuasive.

Applicant asserts that on a broad level, noise is not an issue in a Matsuda regulator circuit to the point where including the noise-free current source taught by Iravani would make sense. Examiner respectfully disagrees. Iravani states that "**Some**

applications require implementing circuits which are so precise in nature, the circuits cannot function properly in the presence of even small amounts of power supply noise." (column 1 lines 16-18, emphasis added). However, the overall objective of Iravani is to reduce noise-sensitive devices from being adversely affected by noise on their power supply (column 2 lines 37-40), which is beneficial to precision circuits. Turning to Figure 1 of Matsuda, the output of the regulator circuit is coupled to internal circuits (Figure 1 and also column 2 lines 20-24). Matsuda further teaches that the arrangement of the regulator circuit is suitable for an application in which the reference voltage is used as a reference voltage of an internal circuit requiring a high precision (column 3 lines 20-21). Therefore, it would have been obvious to one of ordinary skill in the art to use the noise-free current source taught by Iravani in the voltage regulator taught by Matsuda to further increase precision of an internal circuit and would not be an "unneeded additional feature that wastes valuable chip area" as asserted by the Applicant.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to COLLEEN O'TOOLE whose telephone number is (571)270-1273. The examiner can normally be reached on M-F 8:30-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. O./
Examiner, Art Unit 2816

/QUAN TRA/
Primary Examiner, Art Unit 2816